Advances in machine learning for large-scale manufacturing of photonic circuits

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Abstract. Machine learning has opened a new realm of possibilities in photonic circuit design and manufacturing. First, we describe our approach of using deep learning to optimize the multi-dimensional parameter space for hundreds of optical chips on a mask, resulting in homogeneity of performance in high volume applications. Second, we present our approach of using a support vector machine to predict the performance of optical devices by wafer probing. This approach eliminates the expensive and labour-intensive process of optical chip testing, and allows unprecedented control over the fabrication process, including in-situ monitoring of wafer fabrication and real-time process adjustments. The combination of these two approaches paves the way for accelerated adoption of photonics in high volume applications.

1 Introduction

AI and ML have emerged as powerful tools for solving previously intractable problems across various domains, opening up new possibilities for innovation and advancement. Similar to other industries, the photonics industry has begun adopting AI and ML techniques to further both research and deployment of optical technologies. Photonic integrated circuits have grown into a powerful platform that can address the requirements of many of today's demanding applications. The versatile characteristics of photonic integrated circuits [1] make them a desirable solution for realizing multiplexers [2], ultra-dense interferometric architectures [3], as well as long delay lines and K-clocks, leading to their wide adoption not only in telecommunications but also in optical coherence tomography (OCT) and LiDAR systems [4].

Here we present how AI and ML have revolutionized the field of photonic integrated circuit design and manufacturing, allowing mass deployment of high-performance optical chips for communication, advanced vision and imaging applications. We use deep learning to optimize the multi-dimensional design parameter space for hundreds of chips on a production mask. We also use a support vector machine to predict the performance of optical devices by wafer probing. These approaches allow us to achieve an unprecedented control over our fabrication process, leading to consistently high-yields in a high volume manufacturing setting.

2 ML-driven design optimizations

Photonic integrated circuits have been widely used to realize high-performance wavelength division multiplexing (WDM) devices for both telecom and datacom applications [5-6]. A typical 6" silicon wafer contains hundreds of optical chips. Even when these chips are designed to be identical, minute variations in the physical parameters within a wafer can lead to significant performance variations [7]. Fig. 1(a) and 1(b) show the transmission spectra of two chips on the same wafer. Despite the same design parameters, their performance varies vastly due to inevitable variations in the fabrication process. In fact, a wide gradation in performance exists as can be seen if we overlay the spectra of many nominally identical chips from the same wafer, as shown in Fig. 1(c).

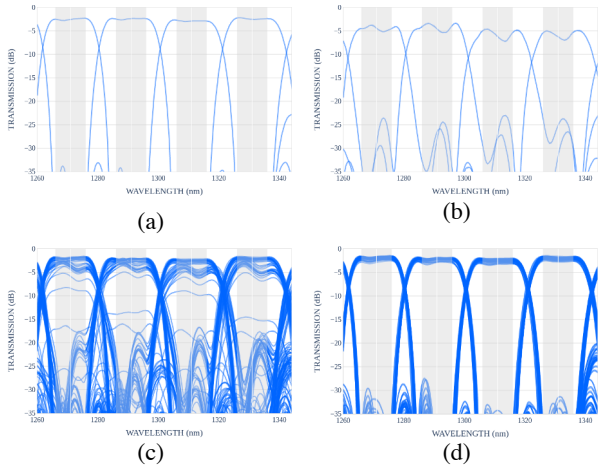

Fig. 1. (a) A transmission spectrum for a multiplexer chip with good performance. (b) A transmission spectrum of a multiplexer chip with poor performance on the same wafer. (c) Variation in the performance of 30 identically-designed chips due to inevitable variations in the fabrication process. (d) Homogeneity of performance achieved after ML was used to optimize the design parameters.

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The high dimensionality of the design and fabrication parameters of photonics chips is ideally suited for deep neural networks that can deduce complex relationships and uncover underlying patterns. We deployed a deep neural network to study the variation in the performance of individual chips, and then inferred the design parameters that characterize a particular photonic chip. The difference between the inferred as-fabricated design parameters and the intended design parameters is captured for each chip on a wafer, and is compensated for in a new optimized production mask. In this new version of the mask, the devices are no longer identical but vary as dictated by the deep neural network model. This approach gives us the ability to achieve homogeneity of performance over hundreds of devices fabricated on a single wafer, despite inevitable variations in the fabrication process, as shown in Fig. 1(d)

3 Prediction of chip performance

Traditionally, the photonics industry has relied on manual chip testing to gauge the performance of the optical chips. This is a time-consuming and labour-intensive process that becomes prohibitively expensive in high volume production.

We have developed a new technology that relies on a wafer probe that collects information to predict the performance of all the chips on the wafer, without requiring individual chip measurements. Fig. 2(a) shows the typical probe spectra collected from 64 locations on the wafer. The goal is to use these spectra to predict the pass / fail distribution of hundreds of chips on a wafer. An example of such distribution, achieved by traditional optical chip testing, is shown in Fig. 2(b). Note that the pass / fail state of an individual chip is determined by a list of about a hundred metrics (per channel insertion loss, passband shape, detuning, crosstalk, etc.), and is therefore a complex multi-dimensional problem.

We trained a support vector machine (SVM) to perform nonlinear binary classification (pass / fail) based on the probe measurement. The prediction of the SVM for a particular wafer is shown in Fig. 2(c). In contrast to the multi-day effort that it takes to characterize the hundreds of optical chips by traditional means and obtain the distribution in Fig. 2(b), the total time required to perform the probe measurement and obtain the predicted map shown in Fig. 2(c) is under 12 minutes. We use the receiver operating characteristic (ROC) curves to cross-validate our binary classifiers and employ an incremental learning algorithm. This approach not only performs the same task in a much more cost- and time-effective way, but also gives us an unprecedented control over our process – since the wafer remains undiced, we are able to perform in-situ monitoring of wafer fabrication and introduce real-time adjustments as required.

3 Conclusions

In this work, we have described our use of AI/ML in the field of photonic integrated circuit design and manufacturing. We used a deep neural network multivariate regression model to optimize the individual design parameters of hundreds of optical chips on a mask. We deployed a support vector machine (SVM) to predict the performance of optical chips in multi-dimensional space. The combination of these two approaches brings the power of machine learning to both the design of optical chips and their manufacturing, allowing us to achieve consistently high performing optical chips at large production volumes.

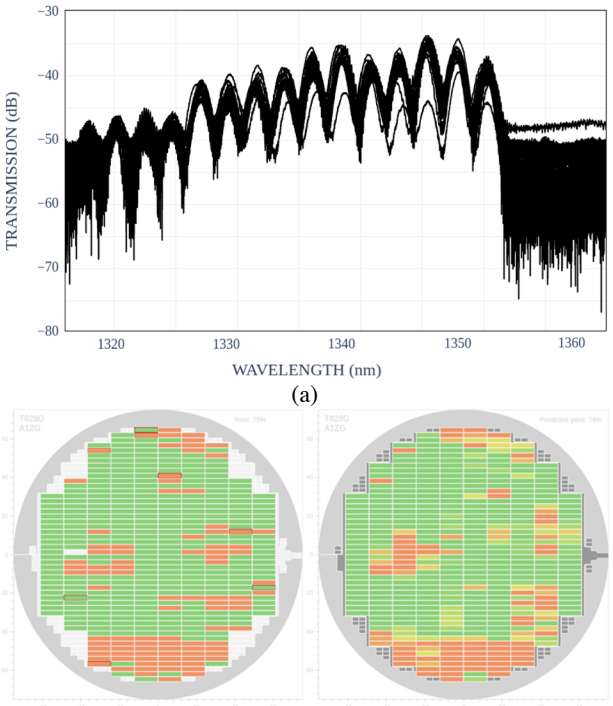

Fig. 2. (a) Typical transmission spectra collected by the wafer probe. (b) Pass (green) / fail (orange) distribution of over 400 chips on a given wafer, obtained by traditional optical chip testing. (c) Pass / fail probability distribution of the same wafer as predicted by an SVM based on a probe measurement.

References

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